REMARKS

Reconsideration of the application is respectfully requested in view of the Applicant's remarks. The Office Action has rejected claims 2, 6, and 8-13.

Rejections under 35 U.S.C. §102(b)

Claims 2, and 8-10 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,961,250 to Snethen ("Snethen"). Applicant respectfully traverses the rejection.

Snethen discloses a method for generating an improved series of test patterns for a logic circuit. In Snethen, a test evaluator determines whether each generated test pattern is to be kept or discarded based on whether it can distinguish between a good machine simulation and a simulated model of a device under test including faults. Col. 16, line 30 – Col. 17, line 5. The Office Action focuses its attention on Snethen's backtracing teachings. However, as will be explained, to the extent backtracing is performed in Snethen, it is not the same as the backtracing required by the pending claim.

Applicant initially notes that in Snethen, the backtracing is performed to determine desired changes to a test pattern applied to primary inputs of a simulated logic network, such that a specific fault for a selected logic block in the simulated logic network can be tested. The backtracing disclosed in Snethen is performed to propagate desired logic values backward from the inputs of the selected logic block to the primary inputs, in order to determine the desired changes to the test pattern applied at the primary inputs. Snethen, Col. 2, lines 58-62. Applicant also notes that to determine a desired test pattern, it may be necessary to perform the backtracing disclosed in Snethen several times to determine a test pattern. Each backtracing step in Snethen changes the test pattern signal applied to one of the primary inputs, and therefore, multiple backtracing steps must be preformed if the test pattern signal must be changed for more than one of the primary inputs. Col. 2, line 62 – col. 3, line 9.

Unlike each of the independent claims 2, 8, 9 and 10, Snethen does not teach "identifying potential faults in the IC that are blocked by the test from being observed at an observable point of said IC by backtracing." Instead, Snethen teaches performing backtracing to "translate[s] the given logic block and value into a required value on some primary input." Col. 18, lines 53-55. If a primary input is reached while the backtracing is being performed in Snethen, "then a new input pattern is derived from the previous one [input pattern] simply by inverting the value on that input." Col. 18, lines 60-62. Thus, the backtracing in Snethen is performed to propagate logic values backward from the logic block towards the primary inputs, and is therefore different from the backtracing recited in claims 2 and 8.

Applicant also notes that Snethen does not teach " performing a good machine simulation on the IC with the test to obtain values of each internal node of the IC." Snethen performs the good machine simulation on a 3-valued simulated reference model of the logic network to be tested. Col. 9, lines 31-37, and Fig. 7. Unlike what is required by the claims, the 3-valued simulated reference model is *not* the integrated circuit that is being tested. Instead, as disclosed in Snethen, the good circuit model is a logic circuit that is separate and distinct from the circuit to be tested. Col. 10, line 65 – Col. 11, line 36, Figures 9, 9A-C, 10A, and 10B. Therefore, Snethen does not disclose performing a good machine simulation *on the IC*, as required by claims 2, 8, 9, and 10. Moreover, in the 2-valued simulated reference model disclosed in Snethen, each signal of the circuit to be tested is represented using two bits in the 3-valued logic system. Col. 10, lines 65-68, and Fig. 9. The 3-valued simulation of Snethen generates the two bit values for each signal as represented in the 3-valued logic system. Applicant respectfully submits that the two bit values for each signal obtained from the circuit to be tested are not the *values of each internal node of the IC*, which is required by claims 2 and 8.

In addition, Snethen does not teach backtracing "in a single detection pass", as is required by claims 2, 8, 9, and 10. In stead, Snethen discloses that "the particular test sequence required at the primary inputs, for this propagation, is obtained by iterative backtracing." Col. 25, lines

60-65. The backtracing step in Snethen is performed several times, with each backtracing step changing a signal values at only one of the primary inputs, until a desired test pattern to be applied to the primary inputs is determined. Col. 2, line 65 – Col. 3, line 5. The backtracing in Snethen must be performed iteratively, and is therefore different from the backtracing performed in a single detection pass recited in claims 2, 8, 9, and 10.

Finally, Applicant notes that Snethen does not disclose backtracing in a single detection pass *through memory elements*. Snethen only discloses performing the disclosed backtracing for logic gates Figures 3, 3A-H, and associated text. Applicant respectfully submits that Snethen contains no teachings relating to backtracing through memory elements. That this is the case is demonstrated by the fact that the Office Action made no attempt to show where Snethen discloses such a feature.

Based on the forgoing, Applicant respectfully submits that claims 2, 8, 9, and 10 are allowable over Snethen.

Rejections Under 35 U.S.C. §103

Claims 6 and 11-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Snethen in view of U.S. Patent No. 5,896,401 to Abramovici et al ("Abramovici"). Applicant respectfully traverses the rejection. In accordance with M.P.E.P. § 2142, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met." (M.P.E.P. § 2143.) First, some suggestion or motivation in the prior art references or in the knowledge of one of ordinary skill in the relevant art must exist to modify or combine the references. Second, if the references are combined, a reasonable expectation of success must be shown. Then, finally, all of the claim limitations must be taught or suggested by one reference or a combination of references. To establish a *prima facie* case of obviousness based on a single reference that does not teach all the elements of a claim, the Examiner must provide a rationale for modifying the teachings of the reference. See

In re Kotzab, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000), *citing*, *B.F. Goodrich Co. v. Aircraft Breaking Sys. Corp.*, 72 F.3d 1577, 1582, 37 U.S.P.Q.2d 1314, 1318 (Fed. Cir.1996).

Abramovici discloses a fault simulator for a digital combinational circuit that uses three distinct models of the digital combinational circuit – a good circuit model, a faulty circuit model, and a backward network. Col 5, lines 1-7 and Fig. 5. The Office Action focuses its attention on Abramovici's backtracing teachings. However, as will be explained, the backtracing taught by Abramovici is not the same as the backtracing required by each of the pending claims.

Applicant initially notes that in Abramovici, the backtracing is performed using both the good circuit model *and* the backward network model. The good circuit model and the backward network model disclosed in Abramovici are two different logic circuits, neither of which are the same as the circuit to be tested. Col. 3, lines 48-54. In other words, the backtracing performed by Abramovici is *not* performed on the actual circuitry in the integrated circuit being tested.

In Abramovici, the good circuit model is a model of the circuit to be tested in a 3-valued logic system. In order to generate the good circuit model, each element of the circuit to be tested is mapped into a logic circuit that models the corresponding element in the 3-valued logic system. Thus, Abramovici discloses performing a 3-valued good machine simulation using the good circuit model *that was generated by substituting library circuit elements for actual circuits found on the integrated circuit being tested.* As Abramovici teaches, each signal of the circuit to be tested is represented by two bits in the 3-valued logic system. Col. 5, lines 9-11.[1]

In Abramovici, backtracing is performed using a backward network *model* that receives the results of the 3-valued logic simulation performed on the good circuit *model*, which determines the critical nodes of the circuit to be tested. The backward network *model* has one primary input for every output of the circuit to be tested and one primary output for every input of the circuit to be tested. The backward network *model* is a logic circuit that calculates the

[1] In the 3-valued logic system, each signal A is represented using two bits A0 and A1. When A0 is 1, A has the value "0" or "x." When A1 is 1, A has the value "1" or "x." Finally, when A0 and A1 are both 1, A has the unknown value "x." Col. 5, lines 11-27 and Fig. 6(a-c).

criticality values for inputs of every logic gate in the circuit to be tested, where the outputs of the logic gate is critical. Col. 5, lines 39-52, and Fig. 9. The backward network model is *not* the integrated circuit that will be tested.

Unlike each of the independent claims 2 and 8, Abramovici does not teach " performing a good machine simulation on the IC with the test to obtain values of each internal node of the IC." As discussed above, Abramovici performs a 3-valued good machine simulation using a good circuit model of the circuit to be tested. Unlike what is required by the claims, the good circuit model is *not* the integrated circuit that is being tested. Instead, as discussed, the good circuit model is a logic circuit that is separate and distinct from the circuit to be tested. Therefore, Abramovici does not disclose performing a good machine simulation *on the IC*, as required by claims 2 and 8. Moreover, as discussed above, in the good circuit model disclosed in Abramovici, each signal of the circuit to be tested is represented using two bits in the 3-valued logic system. The good machine simulation of Abramovici generates the two bit values for each signal as represented in the 3-valued logic system. Applicant respectfully submits that the two bit values for each signal obtained from the circuit to be tested are not the *values of each internal node of the IC*, which is required by claims 2 and 8.

Thus, unlike each of the independent claims 2 and 8, Abramovici does not teach "backtracing, in a single detection pass, through logic gates and memory elements of the IC, starting at each observable node," where the backtracing is "based on outputs of said logic gates and memory elements," and where the outputs are "obtained from said good machine simulation." In fact, as discussed, the good circuit model, and the backward network disclosed in Abramovici are combinational circuits *distinct from the logic gates of the IC*. Figs. 6(b), 6(c), 9 and accompanying text. Moreover, as discussed, the good circuit model in Abramovici is a model that performs 3-valued logic simulation. As discussed above, the 3-valued logic simulation is performed using a combinational circuit that is not the same as the logic gates of the IC. Therefore, the good machine simulation in Abarmovici is not performed on the IC, and

the backtracing in Abramovici is not based on "outputs of said logic gates and memory elements" of the IC. Abramovici also does not teach "backtracing, in a single detection pass, through logic gates and memory elements of the IC" because the backward network used to determine critical nodes in Abramovici is not the same as the logic gates of the IC.

Finally, Applicant notes that Abramovici does not disclose backtracing in a single detection pass *through memory elements*. Abramovici only discloses generation of the good circuit model and the backward network model for AND gates, OR gates, and inverters. Col. 5, line 53 - Col. 6, line 12 and Fig. 9. Applicant respectfully submits that Abramovici contains no teachings relating to backtracing through memory elements. That this is the case is demonstrated by the fact that the Office Action made not attempt to show where Abramovici discloses such a feature.

Claim 6 depends from claim 2, claim 11 depends from claim 8, and claims 12-13 depend either directly or indirectly from claim 9. As discussed above, to the extent backtracing is performed in Snethen, it is not the same as the backtracing required by the pending claims. In addition, as discussed above, the backtracing disclosed in Abramovici is also different from the backtracing required in the pending claims. Applicant respectfully submits that neither Snethen nor Abramovici, either alone or in combination, teach or suggest any of the limitations discussed above, and therefore, these claims are allowable.

Applicant would also like to note that the Attorney Docket No. was changed when the current attorney took over prosecution of this matter. Applicant requests that the Patent Office change their records to reflect this new reference number which is 700693-4011.

Conclusion

In view of the foregoing, Applicant respectfully submits that this application is in condition for allowance, which is respectfully requested. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would

be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (949) 567-6700. If there are any additional fees required, please charge Deposit Account No. 15-0665.

Respectfully submitted,

Orrick, Herrington & Sutcliffe LLP

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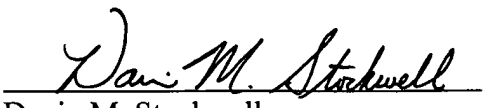
By: 

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